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10/004,458	10/23/2001	Thomas Fung	BRCMP017/BP2054	6843

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EXAMINER	
POPHAM, JEFFREY D	
ART UNIT	**PAPER NUMBER**
2137	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,458	FUNG ET AL.	
	Examiner	Art Unit	
	Jeffrey D. Popham	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-42 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-42 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 October 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 20021028,20030121.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Remarks

Claims 1-42 are pending.

Claim Objections

1. Claims 11, 12, 18, 19, 24, 25, 27, 31, 35, and 39 are objected to under 37 CFR 1.75(a) because of the following informalities:

- Claims 11, 12, and 24, line 2 recite the limitation "the processing engine". There are two processing engines which this could refer to, so for purposes of prior art rejection, it has been construed as "the processing engines".
- Claim 18, line 2 recites the limitation "the younger control record". There is insufficient antecedent basis for this limitation in the claims. For purposes of prior art rejection, it has been construed as "the first control record".
- Claim 19, line 4: "a second interrupt indicator" should be "the second interrupt indicator".
- Claims 27 and 35, line 6: "associated with second interrupt" should be "associated with a second interrupt".
- Claims 27 and 25, lines 8 and lines 8-9, respectively: "a first interrupt" and "the first data block" should be "a second interrupt" and "the second data block", respectively.

- Claims 31 and 39, line 2 recite the limitation "the older data block". There is insufficient antecedent basis for this limitation in the claims. For purposes of prior art rejection, it has been construed as "the second data block".

Appropriate correction is required.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- 500 (history buffer).

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- Figure 3: 309, 331

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the

changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 2, 8-16, and 22-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson et al. ("Context-Agile Encryption for High Speed Communication Networks", Computer Communications Review, Association for Computing Machinery, Vol. 29, No. 1, January 1999, pp. 35-49) in view of Short et al. (U.S. Patent 5,708,814).

Regarding Claim 1,

Pierson et al. disclose a method for processing data using a plurality of processing engines, the method comprising:

Processing first data associated with an older control record in a first processing engine (Pages 44-45, section 5.1.4; and Figure 2);

Processing second data associated with a younger control record in a second processing engine (Pages 44-45, section 5.1.4; and Figure 2); and

Synchronization control to make sure that the younger data is not sent to the CPU before the older data (Pages 44-45, sections 5.1.4 and 5.1.5; and Figure 2);

But do not disclose the use of interrupts.

Short et al., however, disclose collapsing a first interrupt indicator associated with the younger control record onto the older control record (Column 3, line 50 to Column 4, line 6). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt controller of Short et al. into the high speed crypto system of Pierson et al. in order to reduce interrupt processing overhead on the external processor as well as increase both throughput and responsiveness of the system (Column 1, line 51 to Column 2, line 4).

Regarding Claim 2,

Pierson et al. disclose that the first processing engine is a public key engine (Pages 46-48, section 5.2).

Regarding Claim 8,

Pierson et al. disclose that the older control record comprises a reference to data (Page 47, section 5.2.1.1).

Regarding Claim 9,

Pierson et al. disclose that the older control record comprises a reference to an operation to be performed on data (Page 47, section 5.2.1.1).

Regarding Claim 10,

Pierson et al. disclose writing processed data to a memory associated with a host (Page 41, section 5.1.1).

Regarding Claim 11,

Pierson et al. disclose that the host is an external processor coupled to the processing engines (Page 41, section 5.1.1).

Regarding Claim 12,

Pierson et al. disclose that the external processor is coupled to the processing engines through a scheduler (Pages 44-45, sections 5.1.4 and 5.1.5; and Figure 2).

Regarding Claim 13,

Pierson et al. disclose that the data can be output from the crypto accelerator when processing of the older control record has been completed (Page 41, section 5.1.1; and Page 45, section 5.1.5), but not that there is an interrupt generated for this notification.

Short et al., however, disclose generating an interrupt when processing of the control records has been completed (Column 3, line 50 to Column 4, line 6).

Regarding Claim 14,

Short et al. disclose that the external processor reads the processed data when the interrupt is generated (Column 4, lines 23-41).

Regarding Claim 15,

Pierson et al. disclose a cryptography accelerator, comprising:

An interface coupled to an external processor and memory associated with the external processor (Pages 41-45, section 5.1; and Figure 2);

A first processing engine coupled to the interface, the first processing engine configured to receive a first control record from the external processor (Pages 44-45, section 5.1.4; and Figure 2);

A second processing engine coupled to the interface, the second processing engine configured to received a second control record from the external processor (Pages 44-45, section 5.1.4; and Figure 2);

But do not disclose a history buffer containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record.

Short et al., however, disclose a history buffer containing information associated with the first and second control records including a first interrupt indicator associated with the first control record and a second interrupt indicator associated with the second control record (Column 3, line 50 to Column 4, line 6). It would have been obvious to

one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt controller of Short et al. into the high speed crypto system of Pierson et al. in order to reduce interrupt processing overhead on the external processor as well as increase both throughput and responsiveness of the system (Column 1, line 51 to Column 2, line 4).

Regarding Claim 16,

Pierson et al. disclose that the first processing engine is a public key engine (Pages 46-48, section 5.2).

Regarding Claim 22,

Pierson et al. disclose that the second control record comprises a reference to data (Page 47, section 5.2.1.1).

Regarding Claim 23,

Pierson et al. disclose that the second control record comprises a reference to an operation to be performed on data (Page 47, section 5.2.1.1).

Regarding Claim 24,

Pierson et al. disclose that the external processor is coupled to the processing engines through a scheduler (Pages 44-45, sections 5.1.4 and 5.1.5; and Figure 2).

Regarding Claim 25,

Pierson et al. disclose that the data can be output from the crypto accelerator when processing of the older control record has been

completed (Page 41, section 5.1.1; and Page 45, section 5.1.5), but not that there is an interrupt generated for this notification.

Short et al., however, disclose that an interrupt is generated when processing of the control records has been completed (Column 3, line 50 to Column 4, line 6).

Regarding Claim 26,

Short et al. disclose that the external processor reads the processed data when the interrupt is generated (Column 4, lines 23-41).

5. Claims 3-7, 17-21, and 27-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pierson et al. in view of Short et al., further in view of Yamaura (U.S. Patent 6,175,890).

Regarding Claim 3,

Pierson et al. do not disclose that collapsing the first interrupt indicator associated with the younger control record onto the older control record comprises determining that the first interrupt indicator is enabled.

Short et al., however, disclose collapsing the first interrupt indicator associated with the younger control record onto the older control record (Column 3, line 50 to Column 4, line 6), but Pierson et al. as modified by Short et al. does not disclose the enabling of interrupts.

Yamaura, however, discloses determining that the first interrupt indicator is enabled (Column 1, lines 12-30; and Column 4, line 59 to

Column 5, line 10). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the high speed crypto system of Pierson et al. as modified by Short et al. in order to efficiently restore data when it is to be sent to the external processor (Column 2, lines 28-33).

Regarding Claim 4,

Pierson et al. disclose that, when the younger control record completes processing before the second control record, the younger control record will need to be delayed from being output until the processing of the older control record is complete (Page 45, section 5.1.5.3), but do not disclose that this is done via interrupts.

Short et al., however, disclose that collapsing the first interrupt indicator onto the older control record further comprises delaying the generation of an interrupt associated with the younger control record (Column 3, line 50 to Column 4, line 6).

Regarding Claim 5,

Short et al. disclose that collapsing the first interrupt indicator associated with the younger control record onto the older control record further comprises moving the first interrupt indicator associated with the younger control record onto a second interrupt indicator associated with the older control record (Column 4, lines 7-22).

Regarding Claim 6,

Short et al. disclose collapsing the first interrupt indicator associated with the younger control record onto the older control record (Column 3, line 50 to Column 4, line 6), but Pierson et al. as modified by Short et al. does not disclose setting the first interrupt indicator associated with the first control record to disabled.

Yamaura, however, discloses setting the first interrupt indicator associated with the younger control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 7,

Yamaura discloses setting the second interrupt indicator associated with the older control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 17,

Pierson et al. disclose synchronization control to make sure that the younger data does not produce an interrupt to the CPU before the older data (Pages 44-45, sections 5.1.4 and 5.1.5; and Figure 2), but do not disclose collapsing of interrupts.

Short et al., however, disclose that the history buffer is configured to collapse the first interrupt indicator associated with the first control record onto the second interrupt indicator associated with the second control record (Column 3, line 50 to Column 4, line 6), but do not disclose the enabling of interrupts.

Yamaura, however, discloses the enabling of interrupts (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the high speed crypto system of Pierson et al. as modified by Short et al. in order to efficiently restore data when it is to be sent to the external processor (Column 2, lines 28-33).

Regarding Claim 18,

Pierson et al. disclose that, when the first control record completes processing before the second control record, the first control record will need to be delayed from being output until the processing of the second control record is complete (Page 45, section 5.1.5.3), but do not disclose that this is done via interrupts.

Short et al., however, disclose that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises delaying the generation of an interrupt associated with the first control record (Column 3, line 50 to Column 4, line 6).

Regarding Claim 19,

Short et al. disclose that collapsing the first interrupt indicator associated with the first control record onto the second control record further comprises moving the first interrupt indicator associated with the

first control record onto the second interrupt indicator associated with the second control record (Column 4, lines 7-22).

Regarding Claim 20,

Short et al. disclose collapsing the first interrupt indicator associated with the first control record onto the second control record (Column 3, line 50 to Column 4, line 6), but Pierson et al. as modified by Short et al. does not disclose setting the first interrupt indicator associated with the first control record to disabled.

Yamaura, however, discloses setting the first interrupt indicator associated with the first control record to disabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 21,

Yamaura discloses setting the second interrupt indicator associated with the second control record to enabled (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 27,

Pierson et al. disclose a method comprising:

Receiving and processing a first data block using a first processing engine (Pages 44-45, section 5.1.4; and Figure 2); and

Receiving and processing a second data block using a second processing engine (Pages 44-45, section 5.1.4; and Figure 2); and

Sending both data blocks to an output controller (Page 45, section 5.1.5; and Figure 2);

But do not disclose the use of interrupts.

Short et al., however, disclose generating a single interrupt when multiple data blocks are ready to be output to the external processor via multiple interrupt indicators (Column 3, line 50 to Column 4, line 6). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt controller of Short et al. into the high speed crypto system of Pierson et al. in order to reduce interrupt processing overhead on the external processor as well as increase both throughput and responsiveness of the system (Column 1, line 51 to Column 2, line 4).

Short et al. do not disclose the enabling of interrupts.

Yamaura, however, discloses the enabling of interrupts (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the interrupt handling method of Yamaura into the high speed crypto system of Pierson et al. as modified by Short et al. in order to efficiently restore data when it is to be sent to the external processor (Column 2, lines 28-33).

Regarding Claim 35,

Claim 35 is a device claim that corresponds to method claim 27 and is rejected for the same reasons.

Regarding Claim 28,

Pierson et al. disclose that the first and second processing engines are public key engines (Pages 46-48, section 5.2).

Regarding Claim 36,

Claim 36 is a device claim that corresponds to method claim 28 and is rejected for the same reasons.

Regarding Claim 29,

Pierson et al. disclose that the first data block is referenced in a first control record (Page 47, section 5.2.1.1).

Regarding Claim 37,

Claim 37 is a device claim that corresponds to method claim 29 and is rejected for the same reasons.

Regarding Claim 30,

Pierson et al. disclose that the first control record contains information on an operation to perform on the first data block (Page 47, section 5.2.1.1).

Regarding Claim 38,

Claim 38 is a device claim that corresponds to method claim 30 and is rejected for the same reasons.

Regarding Claim 31,

Pierson et al. disclose that the data can be output from the crypto accelerator when processing of the second data block has been completed (Page 41, section 5.1.1; and Page 45, section 5.1.5), but not that there is an interrupt generated for this notification.

Short et al., however, disclose generating a single interrupt when processing of the data blocks has been completed (Column 3, line 50 to Column 4, line 6).

Regarding Claim 39,

Claim 39 is a device claim that corresponds to method claim 31 and is rejected for the same reasons.

Regarding Claim 32,

Short et al. disclose that the first interrupt indicator associated with the first data block is collapsed onto the second interrupt indicator associated with the second data block (Column 3, line 50 to Column 4, line 6).

Regarding Claim 40,

Claim 40 is a device claim that corresponds to method claim 32 and is rejected for the same reasons.

Regarding Claim 33,

Short et al. disclose collapsing the first interrupt indicator (Column 3, line 50 to Column 4, line 6), but not the disabling of interrupts.

Yamaura, however, discloses the disabling of interrupts (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding claim 41,

Claim 41 is a device claim that corresponds to method claim 33 and is rejected for the same reasons.

Regarding Claim 34,

Short et al. disclose collapsing the first interrupt indicator (Column 3, line 50 to Column 4, line 6), but not the enabling of interrupts.

Yamaura, however, discloses the enabling of interrupts (Column 1, lines 12-30; and Column 4, line 59 to Column 5, line 10).

Regarding Claim 42,

Claim 42 is a device claim that corresponds to method claim 34 and is rejected for the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey D. Popham whose telephone number is (571)-272-7215. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571)272-3865. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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